UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/306,813	05/07/1999	YOSHINORI KUNO	P99.0372	3991

33448 7590 06/03/2004

ROBERT J. DEPKE LEWIS T. STEADMAN
HOLLAND & KNIGHT LLC
131 SOUTH DEARBORN
30TH FLOOR
CHICAGO, IL 60603

EXAMINER	
MISLEH, JUSTIN P	

ART UNIT	PAPER NUMBER
2612	15

DATE MAILED: 06/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/306,813	KUNO ET AL.	
	Examiner	Art Unit	
	Justin P Misleh	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 May 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 17 March 2004 have been fully considered but they are not persuasive.

2. The Applicant's presents a point of view that does not stress features in the claim language that are patentable over the prior rather the Applicant's point of view stresses distinctions between the present invention and the prior art. Therefore, regardless of whether actual distinctions that may or may not exist, the claim language is broad and thus, the prior art meets all the features of the claims as will become evident below.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. **Claim 3** is rejected under 35 U.S.C. 102(b) as being anticipated by Endo et al.

Endo et al. disclose, as shown in figure 2, an interline transfer type CCD image sensor (10) wherein a plurality of image sensing elements (PD) are arranged in an array of rows and columns wherein a plurality of vertical transfer registers (VT) are disposed between each column. Connected to the same one end of the plurality of vertical transfer registers (VT) is a single horizontal transfer register (HT) wherein connected to the end of the single horizontal transfer register (HT) is a floating diffusion output amplifier (OA). In addition, connected to other same one end of the plurality of vertical transfer registers (VT) is a single drain register (SD). According to Endo et al., as stated in column 6 (lines 9 – 30), the CCD image sensor (10) is of a multi-layered type wherein excess charges are swept out by means of the single drain register (SD) during an integration period and then the captured charges are read out by means of the single horizontal transfer register (HT) after the integration period. The CCD image sensor (10) requires eight driving pulses for operation of which six of those driving pulses (bg, V1, V2, V3, V4, and sg) are provided by means of a timing pulse generator (74), as stated in columns 5 (lines 65 – 68) and 6 (lines 1 – 8). Four of the six driving pulses (V1 – V4, herein referred as CCD driving pulses) are driving pulses for the image sensing elements (PD) and vertical transfer registers (VT). Endo et al. provides a multi-layered CCD image sensor with two distinct modes of operation wherein during a first mode of operation, the timing system includes the timing pulse generator (74) and is arranged as shown in figure 2 and during a second mode of operation the timing system includes the timing pulse generator (152) and is arranged as shown in figure 5.

In the first mode of operation, the CCD driving pulses (V1 – V4) are four distinctly phased clock pulses and operate in a well-known fashion, as is shown in figures 6A – 6D. In the second mode of operation, the first two CCD driving pulses (V1 and V2) are switched to in-

phase clocked offset pulses (offset by predetermined fixed potentials Va and Vb; see column 9, lines 12 – 26) and the remaining two CCD driving pulses (V3 and V4) are switched to out-of-phase clocked offset pulses (offset by predetermined fixed potentials Vc and Vd; see column 9, lines 35 – 44), as shown in figures 5 and 7A – 7D. To switch between the first mode (figures 6A – 6D) and the second mode (figures 7A – 7D), switching circuits (160, 162, 164, and 166) are provided to switch the CCD driving pulses (V1 – V4) to in-phase and out-of-phase clocked offset pulses (offset by predetermined fixed potentials Va – Vd), respectively, from four distinctly phased clock pulses.

6. For **Claim 3**, Endo et al. disclose a method for driving the horizontal read-out (see explanation below) of a solid state image pickup device provided with a plurality of photoelectric converter portions (PD) being composed of a plurality of pixels in a row, and plurality of charge transfer portions (VT) for transferring the charges generated in the row of pixels in the plurality of photoelectric converter portions, wherein,

a switch circuit (figure 5; more specifically 160, 162, 164, and 166) selects between two modes (first mode and second mode), comprising:

a first mode (see description above and figures 6A – 6D) in which the switch circuit passes drive pulses (V1 – V4) generated by a pulse generator (154) to the charge transfer portions (VT), or

a second mode (see description above and figures 5 and 7A – 7D) in which the switch circuit replaces all of the drive pulses (V1 – V4) with either a predetermined fixed potential (offset by predetermined fixed potentials Va – Vd, respectively) or a floating level (see

explanation below), wherein the switching over is performed independently from signals of the pulse generator (154).

The preamble of the claim recites a method for driving the horizontal read-out of a solid state image pickup device; however the body of the claim is silent with respect to horizontal read-out. The body of the recites, at least, a plurality of photoelectric converter portions being composed of a plurality of pixels in a row, and plurality of charge transfer portions for transferring the charges generated in respective rows of pixels in the plurality of photoelectric converter portions; however, no relation is given to the horizontal read-out of a solid state image pickup device. For these reasons, the Examiner gives the preamble no patentable weight. The Examiner's position is supported in the MPEP.

As stated in the MPEP § 2111.02 (please see also Kropa v. Robie, 187 F.2d 150, 152, 88 USPQ 478, 481 – CCPA 1951), if the preamble of the claim neither recites the limitations of the claim nor is necessary to give life, meaning, and vitality to the claim; then the preamble of the claim is not served to further define the structure of the claim. Thus, the preamble of the claim is not given any patentable weight since the preamble of the claim neither recites the limitations of the claim nor is necessary to give life, meaning, and vitality to the claim.

Again, in the second mode of operation, the first two CCD driving pulses (V1 and V2) are switched to in-phase clocked offset pulses (offset by predetermined fixed potentials Va and Vb; see column 9, lines 12 – 26) and the remaining two CCD driving pulses (V3 and V4) are switched to out-of-phase clocked offset pulses (offset by predetermined fixed potentials Vc and Vd; see column 9, lines 35 – 44), as shown in figures 5 and 7A – 7D. In addition, the switch circuit selection is dependent upon the mode of operation (i.e. first mode or second mode) and

not the timing pulse generator. Finally, the claim requires either a predetermined fixed potential or a floating level; Endo et al. provides predetermined fixed potentials.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. **Claims 1, 2, and 4** are rejected under 35 U.S.C. 103(a) as being unpatentable over Endo et al.

Endo et al. disclose, as shown in figure 2, an interline transfer type CCD image sensor (10) wherein a plurality of image sensing elements (PD) are arranged in an array of rows and columns wherein a plurality of vertical transfer registers (VT) are disposed between each column. Connected to the same one end of the plurality of vertical transfer registers (VT) is a single horizontal transfer register (HT) wherein connected to the end of the single horizontal transfer register (HT) is a floating diffusion output amplifier (OA). In addition, connected to other same one end of the plurality of vertical transfer registers (VT) is a single drain register (SD). According to Endo et al., as stated in column 6 (lines 9 – 30), the CCD image sensor (10) is of a multi-layered type wherein excess charges are swept out by means of the single drain register (SD) during an integration period and then the captured charges are read out by means of the single horizontal transfer register (HT) after the integration period. The CCD image sensor (10) requires eight driving pulses for operation of which six of those driving pulses (bg, V1, V2,

V3, V4, and sg) are provided by means of a timing pulse generator (74), as stated in columns 5 (lines 65 – 68) and 6 (lines 1 – 8). Four of the six driving pulses (V1 – V4, herein referred as CCD driving pulses) are driving pulses for the image sensing elements (PD) and vertical transfer registers (VT). Endo et al. provides a multi-layered CCD image sensor with two distinct modes of operation wherein during a first mode of operation, the timing system includes the timing pulse generator (74) and is arranged as shown in figure 2 and during a second mode of operation the timing system includes the timing pulse generator (152) and is arranged as shown in figure 5.

In the first mode of operation, the CCD driving pulses (V1 – V4) are four distinctly phased clock pulses and operate in a well-known fashion, as is shown in figures 6A – 6D. In the second mode of operation, the first two CCD driving pulses (V1 and V2) are switched to in-phase clocked offset pulses (offset by predetermined fixed potentials Va and Vb; see column 9, lines 12 – 26) and the remaining two CCD driving pulses (V3 and V4) are switched to out-of-phase clocked offset pulses (offset by predetermined fixed potentials Vc and Vd; see column 9, lines 35 – 44), as shown in figures 5 and 7A – 7D. To switch between the first mode (figures 6A – 6D) and the second mode (figures 7A – 7D), switching circuits (160, 162, 164, and 166) are provided to switch the CCD driving pulses (V1 – V4) to in-phase and out-of-phase clocked offset pulses (offset by predetermined fixed potentials Va – Vd), respectively, from four distinctly phased clock pulses.

9. For **Claim 1**, Endo et al. disclose a solid state image pickup device (10) being provided with a photoelectric converter portion (PD) having a plurality of pixels disposed in rows and columns, a charge transfer portion (VT) for transferring the charges generated in said photoelectric converter portion (PD) and a charge/voltage converter portion (OA) for converting

the charges transferred by said charge transfer portion into voltages comprising: a timing pulse generator portion (154) for generating at least more than one pulse signal (any one of bg, V1, V2, V3, V4, and sg) from among four pulse signals which are; a first pulse signal for driving said charge transfer portion (V1 – V4), a second pulse signal for reading out the charges generated in said photoelectric converter portion (V1 – V4), a third pulse signal for sweeping out the charges generated in said photoelectric converter portion (sg), and a fourth pulse signal for discharging the charges transferred to said charge/voltage converter portion (bg), and a switch circuit (figure 5; more specifically 160, 162, 164, and 166) for selectively replacing all of at least one type of pulse signals (the CCD driving pulse signals V1 – V4 during the above described second mode) of said pulse timing pulse generator (154) with either a predetermined fixed potential (offset by predetermined fixed potentials Va – Vd, respectively) or a floating level (see explanation below) and wherein the switch circuit selection is not dependent upon signals from the timing pulse generator (154).

Again, in the second mode of operation, the first two CCD driving pulses (V1 and V2) are switched to in-phase clocked offset pulses (offset by predetermined fixed potentials Va and Vb; see column 9, lines 12 – 26) and the remaining two CCD driving pulses (V3 and V4) are switched to out-of-phase clocked offset pulses (offset by predetermined fixed potentials Vc and Vd; see column 9, lines 35 – 44), as shown in figures 5 and 7A – 7D. In addition, the switch circuit selection is dependent upon the mode of operation (i.e. first mode or second mode) and not the timing pulse generator. Finally, the claim requires either a predetermined fixed potential or a floating level; Endo et al. provides predetermined fixed potentials.

In conclusion, Endo et al. do not disclose wherein the plurality of pixels are disposed strictly in a row, rather disposed the plurality of pixels are disposed in an array of rows and columns. At the time invention was made, one with ordinary skill in the art would have been motivated to provide the plurality of pixels in a row rather than an array simply because all CCD image sensors require thee exact same timing to operate. Therefore, at the time the invention was made, it would have been obvious to one with ordinary skill in the art to have provided the plurality of pixels in a row rather than an array.

10. As for **Claim 4**, Endo et al. disclose the solid state image pickup device of Claim 1, wherein all of the drive pulse signals are replaced (V1 – V4).

Again, in the second mode of operation, the first two CCD driving pulses (V1 and V2) are switched to in-phase clocked offset pulses (offset by predetermined fixed potentials Va and Vb; see column 9, lines 12 – 26) and the remaining two CCD driving pulses (V3 and V4) are switched to out-of-phase clocked offset pulses (offset by predetermined fixed potentials Vc and Vd; see column 9, lines 35 – 44), as shown in figures 5 and 7A – 7D.

11. For **Claim 2**, Endo et al. disclose a method for driving the horizontal read-out (see explanation below) of a solid state image pickup device provided with a photoelectric converter portion (PD) having a plurality of pixels disposed in an array of rows and columns, a charge transfer portion (VT) for transferring the charges generated in said photoelectric converter portion, a charge/voltage converter portion (OA) for converting the charges transferred by said charge transfer portion into voltages, wherein

in a first mode (see description above), a first pulse signal for driving said charge transfer portion (V1 – V4), a second pulse signal for reading out the charges generated in said

photoelectric converter portion (V1 – V4), a third pulse signal for sweeping out the charges generated in said photoelectric converter portion (sg), and a fourth pulse signal for discharging the charges transferred to said charge/voltage converter portion (bg) are selectively supplied to said solid state image pickup device (selectively supplied by means of switching circuits 160, 162, 164, and 166),

in a second mode (see description above), selectively replacing all of the drive pulse signals (V1 – V4) with either a predetermined fixed potential (offset by predetermined fixed potentials Va – Vd, respectively) or a floating level (see explanation below) and wherein the selective replacement of the drive pulse signals (V1 – V4) is performed independently from any of the pulse signals.

The preamble of the claim recites a method for driving the horizontal read-out of a solid state image pickup device; however the body of the claim is silent with respect to horizontal read-out. The body of the recites, at least, a plurality of photoelectric converter portions being composed of a plurality of pixels in a row, and plurality of charge transfer portions for transferring the charges generated in respective rows of pixels in the plurality of photoelectric converter portions; however, no relation is given to the horizontal read-out of a solid state image pickup device. For these reasons, the Examiner gives the preamble no patentable weight. The Examiner's position is supported in the MPEP.

As stated in the MPEP § 2111.02 (please see also Kropa v. Robie, 187 F.2d 150, 152, 88 USPQ 478, 481 – CCPA 1951), if the preamble of the claim neither recites the limitations of the claim nor is necessary to give life, meaning, and vitality to the claim; then the preamble of the claim is not served to further define the structure of the claim. Thus, the preamble of the claim is

not given any patentable weight since the preamble of the claim neither recites the limitations of the claim nor is necessary to give life, meaning, and vitality to the claim.

Again, in the second mode of operation, the first two CCD driving pulses (V1 and V2) are switched to in-phase clocked offset pulses (offset by predetermined fixed potentials Va and Vb; see column 9, lines 12 – 26) and the remaining two CCD driving pulses (V3 and V4) are switched to out-of-phase clocked offset pulses (offset by predetermined fixed potentials Vc and Vd; see column 9, lines 35 – 44), as shown in figures 5 and 7A – 7D. In addition, the switch circuit selection is dependent upon the mode of operation (i.e. first mode or second mode) and not any of the pulse signals. Finally, the claim requires either a predetermined fixed potential or a floating level; Endo et al. provides predetermined fixed potentials.

Endo et al. do not disclose wherein the plurality of pixels are disposed strictly in a row, rather disposed the plurality of pixels are disposed in an array of rows and columns. At the time invention was made, one with ordinary skill in the art would have been motivated to provide the plurality of pixels in a row rather than an array simply because all CCD image sensors require thee exact same timing to operate. Therefore, at the time the invention was made, it would have been obvious to one with ordinary skill in the art to have provided the plurality of pixels in a row rather than an array.

Conclusion

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Justin P Misleh whose telephone number is 703.305.8090. The Examiner can normally be reached on Monday through Thursday from 7:30 AM to 5:30 PM and on alternating Fridays from 7:30 AM to 4:30 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Wendy R Garber can be reached on 703.305.4929. The fax phone number for the organization where this application or proceeding is assigned is 703.872.9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JPM
May 21, 2004

WENDY R. GARBER
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600